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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,598	07/26/2001	Padmanabha I. Venkitakrishnan	10008009	8711

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EXAMINER	
KNOLL, CLIFFORD H	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 07/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/916,598	VENKITAKRISHNAN ET AL.
	Examiner	Art Unit
	Clifford H Knoll	2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to communication filed 5/12/2004. Currently claims 1-20 are pending.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

Rejection of claim 9 under §112 is withdrawn.

Applicant's arguments regarding interpretation of claim 9 are noted. Claim 1 recites "a plurality of cache units, one of the cache units provided for each one of the processor units". In view of Applicant's arguments, and inasmuch as "cache units are provided for *each one of the processor units*", Examiner interprets the "respective cache" recited in claim 9, to refer to the cache associated with the *particular* processor unit (i.e., "provided for each one of the processor units") that is "configured to provide read data via the bus"

Claim Rejections - 35 USC § 102

Claims 1-4, 7, and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli (US 6587926).

Regarding claim 1, Arimilli discloses the processor units, cache units, embedded RAM (e.g., Figure 1), a cache coherent bus coupled to the processor units and the embedded RAM unit, the bus configured to provide cache coherent snooping commands from the processor units to ensure cache coherency between the cache units for the processors and the embedded RAM unit (e.g., col. 2, lines 1-5).

Regarding claim 2, Arimilli also discloses an input output unit coupled to the bus to provide input and output transactions for the processor units (e.g., col. 5, lines 23-27).

Regarding claim 3, Arimilli also discloses the bus configured to provide split transactions for the processor units coupled to the bus (e.g., col. 5, lines 28-31).

Regarding claim 4, Arimilli also discloses the bus is configured to transfer an entire cache line for the cache units of the processor units (e.g., col. 7, lines 48-50).

Regarding claim 7, Arimilli also discloses support of a symmetric multiprocessing method for the plurality of processor units (e.g., col. 4, lines 49-55).

Regarding claim 9, Arimilli also discloses the processor units are configured to provide read data via the bus when the read data is stored within a respective cache unit (e.g., col. 7, lines 54-56).

Thus are claims 1-4, 7, and 9 rejected.

Claim Rejections - 35 USC § 103

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of standard practice of implementing buses, as further evidenced by Arimilli (US 6571322, hereinafter Arimilli-2).

Regarding claim 5, Arimilli also discloses a system bus, but neglects to mention the particular detail of bus width; however the Examiner takes Official Notice that the 256-bit wide system bus is a standard feature of cache coherent architectures. This is further evidenced by Arimilli-2. Arimilli-2 discloses the bus is 256 bits wide (e.g., col. 9, lines 7-8). It would be obvious to combine a standard bus width with Arimilli because Arimilli discloses a particular cache coherency protocol that is useful with standard system buses. Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Arimilli with the standard system bus width of 256 bits.

This is claim 5 rejected.

Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Arimilli-2.

Regarding claim 5, Arimilli also discloses a system bus, but neglects to mention the particular detail of bus width; however this feature is disclosed by Arimilli-2. Arimilli-2 discloses the bus is 256 bits wide (e.g., col. 9, lines 7-8). A person of ordinary skill in the art would be motivated to combine Arimilli-2 with Arimilli because Arimilli-2 teaches

the improvement of a cache coherent system, such as Arimilli, by accommodating the standard system bus width of 256 bits as a sector that does not need to be invalidated (e.g., col. 5, lines 35-38). Therefore it would be obvious to one of ordinary skill in the art to combine Arimilli-2 with Arimilli at the time the invention was made to obtain the claimed invention.

Thus is claim 5 rejected.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of standard practice of memory implementation, as further evidenced by Miller (6560682).

Regarding claim 6, Arimilli discloses an embedded RAM core, but fails to disclose the detail of using DRAM to implement memory; however the examiner takes Official Notice that the use of a DRAM core is standard embodiment of a RAM memory. This is further evidenced by Miller. Miller discloses the embedded DRAM core (e.g., col. 5, lines 7-10). It would be obvious to combine the DRAM implementation of memory with Arimilli because the embedded DRAM core is a standard means to implement a RAM unit. Therefore it would be obvious to one of ordinary skill in the art to combine a standard memory embodiment with the disclosure of Arimilli.

Thus is claim 6 rejected.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of standard embodiment of a processor, as further evidenced by Bitar (US 6418460).

Regarding claim 8, Arimilli neglects to disclose implementational details of a particular processor core; however the Examiner takes Official Notice that MIPS architecture is a standard processor and is well-known for its implementation in symmetric multiprocessing systems, such as in the system of Arimilli. This is further evidenced by Bitar. Bitar discloses the multi-processor units are compatible with a version of a MIPS processor core (e.g., Figure 2B, col. 13, line 39; and col. 17, lines 13-14 in the context of multiprocessor systems). It would be obvious to combine Arimilli with the standard MIPS architecture, because the use of MIPS architecture is widely known in the implementation of symmetric multiprocessing systems such as the system of Arimilli. Therefore at the time the invention was made, it would be obvious to a person of ordinary skill in the art to combine the MIPS architecture, as evidenced by Bitar, with Arimilli to obtain the claimed invention.

Thus is claim 8 rejected.

Claims 10-13, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of the standard practice of integrating circuits, as further evidenced by Sherburne (2002/0184546).

Regarding claim 10, Arimilli discloses a power supply; a plurality of processor units; a plurality of cache units, one of the cache units provided for each one of the

processor units; an embedded RAM unit for storing instructions and data for the processor units (e.g., Figure 1); a cache coherent bus coupled to the processor units and the embedded RAM unit, the bus configured to provide cache coherent snooping commands from the processor units to ensure cache coherency between the cache units for the processor units and the embedded RAM unit (e.g., col. 2, lines 1-5). Arimilli does not expressly mention a particular embodiment of an integrated circuit die; however the Examiner takes Official Notice that it is manifestly obvious to integrate multi-processing devices for the well-known and well-noted advantages of portability, power consumption, and so forth. This is further evidenced by Sherburne. Sherburne discloses the well-known practice of using highly integrated devices to obtain the advantages of decreased size and weight (e.g., paragraph [0002]). It would be obvious to combine Arimilli with the well-known practice of integration because the practice is standard and the advantages for doing so are well established in areas such as those evidenced by Sherburne, which included multiprocessing systems with cache and embedded memory. Therefore it would be obvious to one of ordinary skill in the art to combine Arimilli with the standard practice of integration.

Regarding claim 11, Arimilli also discloses an input output unit coupled to the bus to provide input and output transactions for the processor units (e.g., col. 5, lines 23-27).

Regarding claim 12, Arimilli also discloses the bus configured to provide split transactions for the processor units coupled to the bus (e.g., col. 5, lines 28-31).

Regarding claim 13, Arimilli also discloses the bus is configured to transfer an entire cache line for the cache units of the processor units (e.g., col. 7, lines 48-50).

Regarding claim 16, Arimilli also discloses support of a symmetric multiprocessing method for the plurality of processor units (e.g., col. 4, lines 49-55).

Regarding claim 18, Arimilli also discloses the processor units are configured to provide read data via the bus when the read data is stored within a respective cache unit (e.g., col. 7, lines 54-56).

Thus are claims 10-13, 16, and 18 rejected.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli and the standard practice of integration, as applied in claim 10 above, further in view of Arimilli-2.

Regarding claim 14, Arimilli also discloses a system bus, but neglects to mention the particular detail of bus width; however this feature is disclosed by Arimilli-2. Arimilli-2 discloses the bus is 256 bits wide (e.g., col. 9, lines 7-8). A person of ordinary skill in the art would be motivated to combine Arimilli-2 with Arimilli because Arimilli-2 teaches the improvement of a cache coherent system, such as Arimilli, by accommodating the standard system bus width of 256 bits as a sector that does not need to be invalidated (e.g., col. 5, lines 35-38). Therefore it would be obvious to one of ordinary skill in the art to combine Arimilli-2 with Arimilli and the well-known practice of integration at the time the invention was made to obtain the claimed invention.

Thus is claim 14 rejected.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli and the standard practice of integration, as applied in claim 10 above, further in view of the standard practice of memory implementation, as further evidenced by Miller.

Regarding claim 15, Arimilli fails to disclose the detail of using DRAM to implement memory; however the examiner takes Official Notice that the use of a DRAM core is standard embodiment of a RAM memory. This is further evidenced by Miller. Miller discloses the embedded DRAM core (e.g., col. 5, lines 7-10). It would be obvious to combine standard implementation practice with Arimilli because the DRAM is a standard means to implement an embedded RAM core. Therefore it would be obvious to one of ordinary skill in the art to combine a standard memory embodiment with the disclosure of Arimilli and the well-known practice of integration.

Thus is claim 15 rejected.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli and the standard practice of integration, as applied in claim 10 above, further in view of a standard processor embodiment, as evidenced by Miller.

Regarding claim 17, Arimilli neglects to disclose implementational details of a particular processor core; however the Examiner takes Official Notice that MIPS architecture is a standard processor for symmetric multiprocessing, such as in the system of Arimilli. This is further evidenced by Bitar. Bitar discloses the processor units are compatible with a version of a MIPS processor core (e.g., Figure 2B, col. 13, line 39; and col. 17, lines 13-14 in the context of multiprocessor systems). It would be obvious

to combine Arimilli with the standard MIPS architecture, because the use of MIPS architecture is standard in the implementation of symmetric multiprocessing systems such as the system of Arimilli. Therefore at the time the invention was made, it would be obvious to a person of ordinary skill in the art to combine the MIPS architecture, a standard embodiment as evidenced by Bitar, with Arimilli and the standard practice of integration to obtain the claimed invention.

Thus is claim 17 rejected.

Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli, in view of standard practice of integration and memory implementation, as evidenced by Sherburne, and further in view of Arimilli-2.

Regarding claim 19, Arimilli discloses and a power supply, a plurality of processor units; a plurality of cache units, one of the cache units provided for each one of the processor units; an embedded RAM core unit for storing instructions and data for the processor units (e.g., Figure 1); a cache coherent bus coupled to the processor units and the embedded RAM core unit, the bus configured to provide cache coherent snooping commands from the processor units to ensure cache coherency between the cache units for the processor units and the embedded RAM core unit (e.g., col. 2, lines 1-5). Arimilli does not expressly mention a particular embodiment of an integrated circuit die and said invention occurring in a portable hand-held device; however the Examiner takes Official Notice that it is manifestly obvious to integrate multi-processing devices for the well-known and well-noted advantages of portability, power

consumption, and so forth. Likewise, the Examiner also takes Official Notice that the use of DRAM as a memory implementation is standard practice. This also is further evidenced by Sherburne. Sherburne discloses the well-known practice of using highly integrated devices rendering the advantages of decreased size and weight (e.g., paragraph [0002]) as well as the manifest advantages of portability in a use such as handheld device (e.g., paragraph [0002]) and also the use of DRAM to implement memory (e.g., Figure 1). It would be obvious to combine Arimilli with the well-known practice of integration because the practice is standard and the advantages for doing so are well established in areas such as those evidenced by Sherburne, which include multiprocessing systems with cache and embedded memory. Likewise the use of DRAM to implement memory as, evidenced by Sherburne, is standard practice. Therefore it would be obvious to one of ordinary skill in the art to combine Arimilli with the standard practice of integration.

Arimilli also discloses a system bus, but neglects to mention the particular detail of bus width; however this feature is disclosed by Arimilli-2. Arimilli-2 discloses the bus is 256 bits wide (e.g., col. 9, lines 7-8). A person of ordinary skill in the art would be motivated to combine Arimilli-2 with Arimilli because Arimilli-2 teaches the improvement of a cache coherent system, such as Arimilli, by accommodating the standard system bus width of 256 bits as a sector that does not necessarily need to be invalidated (e.g., col. 5, lines 35-38). Therefore it would be obvious to one of ordinary skill in the art to combine Arimilli-2 with Arimilli and the well-known practice of integration at the time the invention was made to obtain the claimed invention.

Regarding claim 20, Arimilli also discloses the bus configured to provide split transactions for the processor units coupled to the bus (e.g., col. 5, lines 28-31).

Thus are claims 19 and 20 rejected.

Response to Arguments

Applicant's arguments filed 5/12/2004 have been fully considered but they are not persuasive.

Regarding claim 1, Applicant argues that Arimilli at the cited passage discloses "managing the routing of data access transactions" and is silent on "snooping commands that maintain cache coherency between processor cache units and a RAM unit. Indeed, nowhere in the Arimilli et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that ensure cache coherency" (p. 3); however this interpretation is incorrect. The purpose of cache snooping is precisely to enable cache coherency. Arimilli at the cited passage discloses: "To allow devices snooping the system bus to identify and properly route bus transactions a system address tag that identifies the request source is included within each data access request and returned with each corresponding response" (col. 2, lines 1-5). The invention of Arimilli directly concerns the management of the tags which are part of the cache snooping architecture. The particular embodiment of tag management in Arimilli is not relevant; the cache snooping architecture is.

Thus the rejection of claim 1 is maintained.

Regarding remaining claims, Applicant's argues as supra against Arimilli disclosing providing "cache coherent snooping commands..." (pp. 4-11); however, this is treated supra.

Arimilli is seen to discuss coherency throughout his disclosure, for example: "The information encoded within the returned source path tag enables the response to be properly recognized and processed by intermediate devices as it is routed to the original source device. For example, in a data storage system employing inclusive vertical memory coherency, each memory level from the L1 through system memory must include all data stored within the lower levels" (col. 8, lines 6-12), which clearly exemplifies and establishes the relationship between data tags and snooping to provide cache coherency.

Thus the rejection of the remaining claims is maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 703-305-8656. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk

Khanh Dang
Primary Examiner